

# Hardware Transactional Persistent Memory

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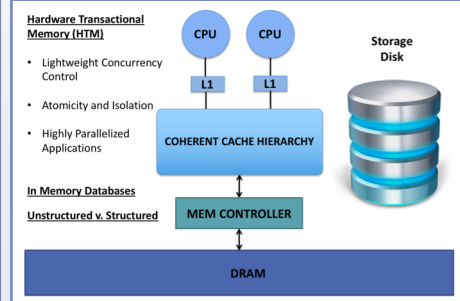
Dr. Peter Varman  
Rice ECE (Advisor)



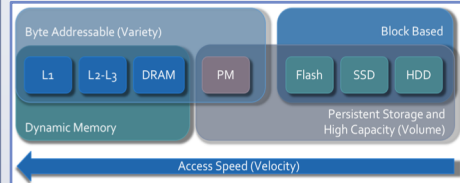
Dr. Kshitij Doshi  
Intel Corporation (Advisor)

## MOTIVATION

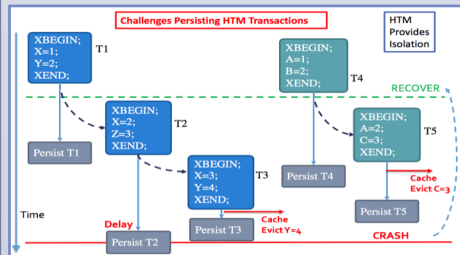
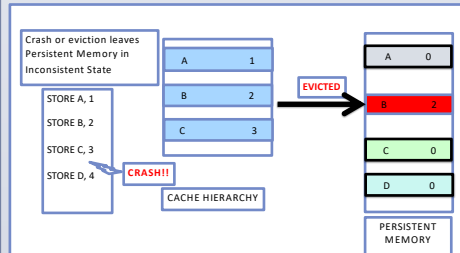
Combine highly parallelized applications utilizing new Hardware Transactional Memory with emerging byte-addressable Persistent Memory



## PERSISTENT MEMORY



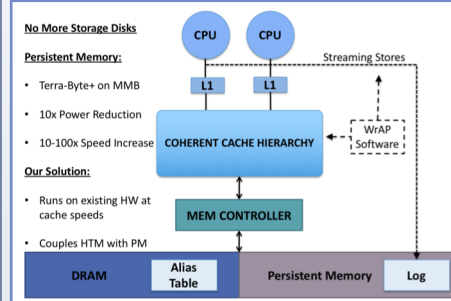
## PERSISTENCE CONSISTENCY



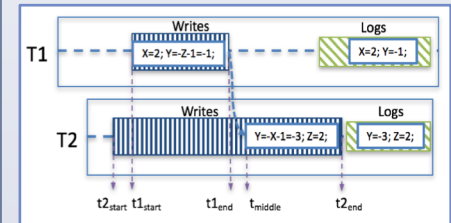
Random cache evictions to PM and delayed logging outside HTM sections involve complex ordering and recovery mechanisms.

## SOFTWARE BASED SOLUTION

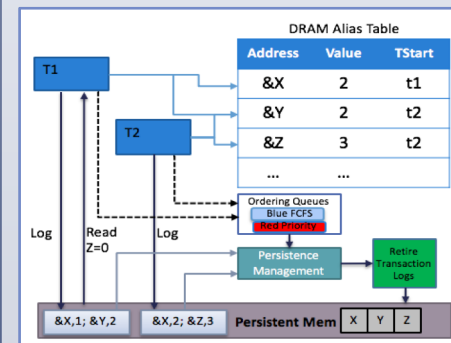
Hardware Transactional Persistent Memory, software based solution couples HTM with Persistent Memory on existing Intel based processors.



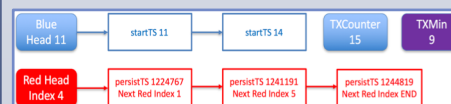
## CONCURRENCY AND LOGGING PHASES



## CATCH CACHE EVICTIONS WITH ALIASING



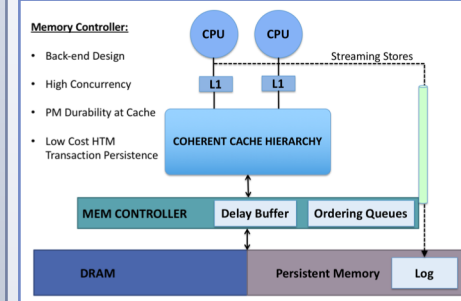
## ORDERING FOR PERSISTENCE



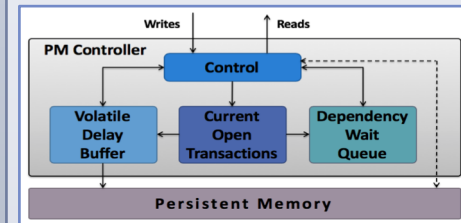
Hardware Transactional Persistent Memory successfully couples HTM with PM using existing processors and memory architecture.

## MEMORY CONTROLLER SOLUTION

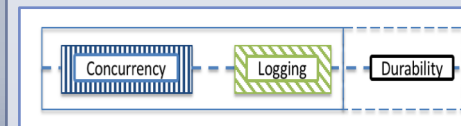
We introduce memory controller support on the back-end without changes to the cache hierarchy or coherency mechanisms for higher performance.



## CONTROLLER TRACKS DEPENDENCIES



## BOTH SOLUTIONS PROVIDE RELAXED DURABILITY



We split a transaction into Concurrency (HTM), Logging, and Durability phases.

A transaction can choose between:

- Relaxed durability for high performance. Transaction will become fully recoverable at some future time.
- Strict durability waits until a transaction is guaranteed to be fully recoverable, all other txns have completed.

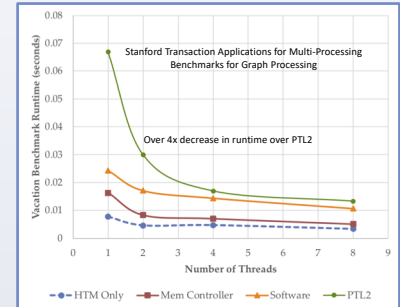
## RELATED WORK

- Failure Atomicity for 64-byte writes and persistent store fences
- PHTM, PyHTM, DUDETM require full hardware changes
- Full cache and battery backup based work
- SCM based file systems, Pmem, BPFs, SCMFS, and others
- Mnemosyne, Full VM system, interception of all reads & writes
- ATLAS, Automatically generates atomic regions; Undo Log

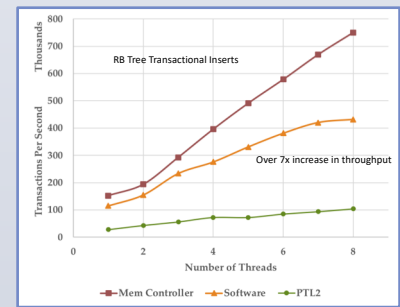
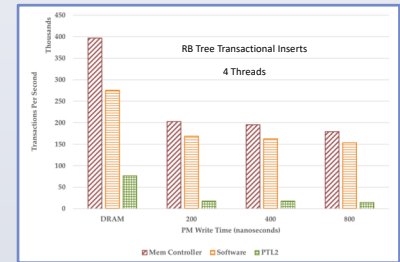
Memory controller support lets transaction operate at near cache and Hardware Transactional Memory speeds with low-cost persistence.

## RESULTS

Our Hardware Transactional Persistence Memory solutions achieve high performance by combining fast HTM for concurrency and PM for storage.



Intel(R) Xeon(R) E5-2650 v4 Processor with 12 cores



## CONCLUSIONS

- Our Hardware Transactional Persistence Memory combines HTM with Persistence Memory without hardware processor or cache changes
- Couples HTM with PM solving cache-evictions, ordering and durability challenges w/o hardware changes
- Achieves near pure HTM (no persistence) performance
- 7x Faster than other persistence methods like PTL2
- Forward work includes IBM POWER implementation